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KEYSIGHT TECHNOLOGIES

Programmer's Reference

Notices

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WARNING

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In This Book

This book is your guide to programming the Keysight Technologies N5393D/E PCI-Express Compliance Application.

- Chapter 1, “Introduction to Programming,” starting on page 7 describes compliance application programming basics.
- Chapter 2, “Configuration Variables and Values,” starting on page 9, Chapter 3, “Test Names and IDs,” starting on page 21, and Chapter 4, “Instruments,” starting on page 51 provide information specific to programming the N5393D/E PCI-Express Compliance Application.

How to Use This Book

Programmers who are new to compliance application programming should read all of the chapters in order. Programmers who are already familiar with this may review chapters 2, 3, and 4 for changes.

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1 Introduction to Programming

Remote Programming Toolkit / 8

This chapter introduces the basics for remote programming a compliance application. The programming commands provide the means of remote control. Basic operations that you can do remotely with a computer and a compliance app running on an oscilloscope include:

- Launching and closing the application.
- Configuring the options.
- Running tests.
- Getting results.
- Controlling when and were dialogs get displayed
- Saving and loading projects.

You can accomplish other tasks by combining these functions.

Remote Programming Toolkit

The majority of remote interface features are common across all the Keysight Technologies, Inc. family of compliance applications. Information on those features is provided in the N5452A Compliance Application Remote Programming Toolkit available for download from Keysight here: www.keysight.com/find/rpi. The N5393D/E PCI-Express Compliance Application uses Remote Interface Revision 3.40. The help files provided with the toolkit indicate which features are supported in this version.

In the toolkit, various documents refer to "application-specific configuration variables, test information, and instrument information". These are provided in Chapters 2, 3, and 4 of this document, and are also available directly from the application's user interface when the remote interface is enabled (View>Preferences::Remote tab::Show remote interface hints). See the toolkit for more information.

2 Configuration Variables and Values

The following table contains a description of each of the N5393D/E PCI-Express Compliance Application options that you may query or set remotely using the appropriate remote interface method. The columns contain this information:

- GUI Location – Describes which graphical user interface tab contains the control used to change the value.
- Label – Describes which graphical user interface control is used to change the value.
- Variable – The name to use with the SetConfig method.
- Values – The values to use with the SetConfig method.
- Description – The purpose or function of the variable.

For example, if the graphical user interface contains this control on the **Set Up** tab:

- Enable Advanced Features

then you would expect to see something like this in the table below:

Table 1 Example Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Set Up	Enable Advanced Features	EnableAdvanced	True, False	Enables a set of optional features.

and you would set the variable remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SetConfig 'EnableAdvanced' 'True'"

C# syntax
```

```
---------
remoteAte.SetConfig("EnableAdvanced", "True");
```

Here are the actual configuration variables and values used by this application:

NOTE Some of the values presented in the table below may not be available in certain configurations. Always perform a "test run" of your remote script using the application's graphical user interface to ensure the combinations of values in your program are valid.

NOTE The file, "ConfigInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 2 Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Confgure	Clock Recovery Delta Time	ClockRecoveryDeltaTime	Fixed, Variable	Select the clock recovery delta time from compliance pattern of 64 zeroes and 64 ones
Confgure	Connection Type	AddinTxConnectionType	1, 2, 3, 4, 5, 6, 7, 8	Identifies the channels to process. For Direct Connect, connect the first channel to the + signal and the second channel to the - signal.
Confgure	Connection Type	ECHostTxConnectionType	1, 2, 3, 4, 5, 6, 7, 8	Identifies the channels to process. For Direct Connect, connect the first channel to the + signal and the second channel to the - signal.
Confgure	Connection Type	ECModuleTxConnectionType	1, 2, 3, 4, 5, 6, 7, 8	Identifies the channels to process. For Direct Connect, connect the first channel to the + signal and the second channel to the - signal.
Confgure	Connection Type	Gen2SystemTxConnectionType	11, 12, 13, 14	(Limited availability*) Identifies the channels to process.
Confgure	Connection Type	Gen3RxConnectionType	1, 2, 3, 4, 5, 6	Identifies the channels to process. For Direct Connect, connect the first channel to the + signal and the second channel to the - signal.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	Connection Type	PresetTxConnectionType	1, 2, 3, 4, 5, 6, 7, 8	Identifies the channels to process. For Direct Connect, connect the first channel to the + signal and the second channel to the - signal.
Confgure	Connection Type	RefClkConnectionType	1, 2, 3, 4, 5, 6, 7, 8	Identifies the channels to process. For Direct Connect, connect the first channel to the + signal and the second channel to the - signal.
Confgure	Connection Type	RxConnectionType	1, 2, 3, 4, 5, 6	Identifies the channels to process. For Direct Connect, connect the first channel to the + signal and the second channel to the - signal.
Confgure	Connection Type	SystemTxConnectionType	1, 2, 3, 4, 5, 6, 7, 8	Identifies the channels to process. For Direct Connect, connect the first channel to the + signal and the second channel to the - signal.
Confgure	Connection Type	TxConnectionType	1, 2, 3, 4, 5, 6, 7, 8	Identifies the channels to process. For Direct Connect, connect the first channel to the + signal and the second channel to the - signal.
Confgure	De-Emphasis Removal	EnableDeEmpRemoval	1.0, 0.0	Enable or Disable De-Emphasis Removal feature for the jitter and eye width measurement of the transmitter test.
Confgure	Deembed Fixture (dB)	Deembed	(Accepts user-defined text), 0.0, -0.50, -1.00, -1.50	Identify the amount of fixture and cable loss in dB. Probe external scaling will be set to compensate. Maximum compensation value is -60dB.
Confgure	Differential clock waveform file name	DiffClkWfmFile	(Accepts user-defined text), None	This variable use to store the directory of the differential clock waveform file.
Confgure	Differential waveform file name	DiffWfmFile	(Accepts user-defined text), None	This variable use to store the directory of the differential data waveform file.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	Gen 2 Ref Clock Transfer Function (Common Clock)	Gen2CommonRefClkTF	H1: 5MHz, 1.0dB peaking | H2: 16MHz, 3.0dB peaking, H1: 8MHz, 3.0dB peaking | H2: 16MHz, 3.0dB peaking	Select the transfer function for Gen 2 reference clock signal.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	Gen 3 Ref Clock Transfer Function (Common Clock)	Gen3CommonRefClkTF	H1: 2MHz, 0.01dB peaking | H2: 2MHz, 0.01dB peaking, H1: 2MHz, 0.01dB peaking | H2: 2MHz, 1.0dB peaking, H1: 2MHz, 0.01dB peaking | H2: 5MHz, 0.01dB peaking, H1: 2MHz, 0.01dB peaking | H2: 5MHz, 1.0dB peaking, H1: 2MHz, 2.0dB peaking | H2: 2MHz, 0.01dB peaking, H1: 2MHz, 2.0dB peaking | H2: 2MHz, 1.0dB peaking, H1: 2MHz, 2.0dB peaking | H2: 5MHz, 0.01dB peaking, H1: 2MHz, 2.0dB peaking | H2: 5MHz, 1.0dB peaking, H1: 4MHz, 0.01dB peaking | H2: 2MHz, 0.01dB peaking, H1: 4MHz, 0.01dB peaking | H2: 2MHz, 1.0dB peaking, H1: 4MHz, 0.01dB peaking | H2: 5MHz, 0.01dB peaking, H1: 4MHz, 0.01dB peaking | H2: 5MHz, 1.0dB peaking, H1: 4MHz, 2.0dB peaking | H2: 2MHz, 0.01dB peaking, H1: 4MHz, 2.0dB peaking | H2: 2MHz, 1.0dB peaking, H1: 4MHz, 2.0dB peaking | H2: 5MHz, 0.01dB peaking, H1: 4MHz, 2.0dB peaking | H2: 5MHz, 1.0dB peaking	Select the transfer function for Gen 3 reference clock signal.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	Gen 3 Ref Clock Transfer Function (Data Clock)	Gen3DataRefClkTF	H1: 2MHz, 0.01dB peaking | H2: 10MHz, 0.5dB peaking, H1: 2MHz, 1.0dB peaking | H2: 10MHz, 0.5dB peaking, H1: 2MHz, 2.0dB peaking | H2: 10MHz, 0.5dB peaking, H1: 2MHz, 0.01dB peaking | H2: 10MHz, 2.0dB peaking, H1: 2MHz, 1.0dB peaking | H2: 10MHz, 2.0dB peaking, H1: 2MHz, 2.0dB peaking | H2: 10MHz, 2.0dB peaking, H1: 4MHz, 0.01dB peaking | H2: 10MHz, 0.5dB peaking, H1: 4MHz, 0.01dB peaking | H2: 10MHz, 2.0dB peaking, H1: 4MHz, 2.0dB peaking | H2: 10MHz, 0.5dB peaking, H1: 4MHz, 2.0dB peaking | H2: 10MHz, 2.0dB peaking, H1: 5MHz, 0.01dB peaking | H2: 10MHz, 0.5dB peaking, H1: 5MHz, 0.01dB peaking | H2: 10MHz, 2.0dB peaking, H1: 5MHz, 1.0dB peaking | H2: 10MHz, 0.5dB peaking, H1: 5MHz, 1.0dB peaking | H2: 10MHz, 2.0dB peaking	Select the transfer function for Gen 3 reference clock signal.
Confgure	Noise Reduction BW, GHz	EBW	0.0, 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9, 8.0E+9, 7.0E+9, 6.5E+9, 6.0E+9, 5.5E+9, 5.0E+9, 4.5E+9, 4.0E+9, 3.5E+9, 3.0E+9, 2.5E+9, 2.0E+9, 1.5E+9, 1.0E+9	(Limited availability*) Specify the noise reduction bandwidth to use for all tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	Num Clock UI	NumClockUI	(Accepts user-defined text), 1000000, 500000, 100000, 50000	This is the number of clock unit intervals processed when calculating clock jitter. For compliance testing, this measurement requires 1,000,000 UI to guarantee the proper bit error rate (10E-6 BER) as specified in the PCI Express Base Specification Rev. 1.1. The allowed values for this control are between 1000 and 3,000,000 UIs.
Confgure	Number of UI	NumUIGen1Test	(Accepts user-defined text), 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3, 100.0E+3, 50.0E+3	This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests.
Confgure	Number of UI	NumUIGen2Test	(Accepts user-defined text), 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3, 100.0E+3, 50.0E+3	This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests.
Confgure	Output Filename	RefClkOutputCSVFilename	(Accepts user-defined text), None, Auto	Output Filename.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	ProbeHead Check	EnableProbeHeadCheck	1.0, 0.0	When ProbeHead check is enabled, the input signal's probe head configuration is verified. This is only done when performing DualPort Testing in Gen2 System Board Test.
Confgure	RJ Bandwidth	RJBW	NARR, WIDE	Select the RJ bandwidth.
Confgure	Rise/Fall Time Measurement Count	RiseFallCount	10.0E+3, 5.0E+3, 2.0E+3, 1.0E+3, 500.0E+0, 200.0E+0	Select the minimum measurement count for each rise time and fall time for the Rise/Fal time measurement with variable threshold.
Confgure	S-Parameter for Add-in Card	AddInSParamFilePath	(Accepts user-defined text)	Stores the s-parameter file path for Add-in card tests.
Confgure	S-Parameter for System Board	SystemSParamFilePath	(Accepts user-defined text)	Stores the s-parameter file path for System board tests.
Confgure	Sample Rate, GSa/s	SRate	80.0E+9, 40.0E+9, 20.0E+9, 10.0E+9, 5.0E+9	(Limited availability*) Specify the sample rate to use for all PCIE 1.0a, PCIE 1.1 , PCIe 2.0 (2.5 GT/s) and Express Card 1.0 tests.
Confgure	Sample Rate, GSa/s	SRate_Gen2	80.0E+9, 40.0E+9, 20.0E+9, 10.0E+9	(Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests.
Confgure	Sample rate, GSa/s	ClockSR	80.0E+9, 40.0E+9, 20.0E+9, 10.0E+9, 5.0E+9, 2.0E+9, 1.0E+9	Select the sample rate to acquire reference clock signal.
Confgure	Show Jitter Filter Plot	ShowJitterFilterPlot	0, 2, 3, 4, 5	Select the clock jitter plot to display. Generating plots will increase test runtime.
Confgure	Signal Check	EnableSignalCheck	1.0, 0.0	When signal check is enabled, the input signal is pre-tested and verified to be within a reasonable range of timing and voltage limits. This can be useful for detecting problems like cabling errors before a test is run.
Confgure	Sine(x)/x Interpolation	SineXInterpolation	ON, OFF, INT1, INT2, INT4, INT8	Sine(x)/x Interpolation.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Confgure	Single ended negative clock waveform file name	ClkDNWfmFile	(Accepts user-defined text), None	This variable use to store the directory of the single ended negative clock waveform file.
Confgure	Single ended negative clock waveform file name	OfflineInput	(Accepts user-defined text), None	This variable use to store the type of offline waveform, "SingleEnded" or "Differential".
Confgure	Single ended negative waveform file name	DNWfmFile	(Accepts user-defined text), None	This variable use to store the directory of the single ended negative data waveform file.
Confgure	Single ended positive clock waveform file name	ClkDPWfmFile	(Accepts user-defined text), None	This variable use to store the directory of the single ended positive clock waveform file.
Confgure	Single ended positive waveform file name	DPWfmFile	(Accepts user-defined text), None	This variable use to store the directory of the single ended positive data waveform file.
Confgure	Stitch Method	StitchMethod	Absolute, Dynamic	Select the method to stitch the waveform for reference clock phase jitter test. Absolute method stitches the waveform based on absolute data. Dynamic method aligns waveform data to have common offset before stitching. This option only applies when Spread Sprectrum Clocking is enabled.
Confgure	Transition Time Threshold	TransitionTimeThreshold	Fixed, Variable	Select the threshold method used to measure transition time.Fixed method applied the same threshold for all edges. Variable method applied threshold based on the previous and the next unit interval.
Confgure	Trigger Pulse Width, s	TrigPulseWidth	8.0E-9, 7.0E-9, 6.0E-9, 5.0E-9	(Limited availability*) Specify the width in second for the Pulse Width Trigger setup.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Run Tests	Event	RunEvent	(None), Fail, Margin < N, Pass	Names of events that can be used with the StoreMode=Event or RunUntil RunEventAction options
Run Tests	RunEvent=Margin < N: Minimum required margin %	RunEvent_Margin < N_MinPercent	Any integer in range: 0 <= value <= 100	Specify N using the 'Minimum required margin %' control.
Set Up	Add-in Card Tests	TestPoint_AddInCard	0.0, 1.0	Select tests peformed at the add-in card interface on the add-in card transmitter path.
Set Up	Clean Clock	persistentCheckBox_Clean	0.0, 1.0	Indicate whether a Clean Clock is used.
Set Up	Data Rate	DataRateOpt	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	Select data rate option for PCIE Gen2 test signal.
Set Up	De-Emphasis Mode	DeEmpOpt	-3.5 dB, -6.0 dB, None	Select de-emphasis level for PCIE Gen2 test signal.
Set Up	Device	DevicePCIErev	PCIE 1.0a, PCIE 1.1, PCIE 2.0, PCIE 3.0, Express Card 1.0	Select the PCI Express device specification to use.
Set Up	Device ID	txtDeviceID	(Accepts user-defined text)	Optional user defined device ID displayed in the test report.
Set Up	Embed Enable Checkbox	OfflineEnable	0.0, 1.0	Select tests peformed at the reference clock interface.
Set Up	Express Card Host	TestPoint_ExpressCardHost	0.0, 1.0	Select tests peformed on Express Card Hosts.
Set Up	Express Card Module	TestPoint_ExpressCardModule	0.0, 1.0	Select tests peformed on Express Card Modules.
Set Up	Lane0	Lane0	0.0, 1.0	Select tests performed at the transmitter package pins.
Set Up	Lane1	Lane1	0.0, 1.0	Select tests performed at the transmitter package pins.
Set Up	Lane10	Lane10	0.0, 1.0	Select tests performed at the transmitter package pins.
Set Up	Lane11	Lane11	0.0, 1.0	Select tests performed at the transmitter package pins.
Set Up	Lane12	Lane12	0.0, 1.0	Select tests performed at the transmitter package pins.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Lane13	Lane13	0.0, 1.0	Select tests performed at the transmitter package pins.
Set Up	Lane14	Lane14	0.0, 1.0	Select tests performed at the transmitter package pins.
Set Up	Lane15	Lane15	0.0, 1.0	Select tests performed at the transmitter package pins.
Set Up	Lane2	Lane2	0.0, 1.0	Select tests performed at the transmitter package pins.
Set Up	Lane3	Lane3	0.0, 1.0	Select tests performed at the transmitter package pins.
Set Up	Lane4	Lane4	0.0, 1.0	Select tests performed at the transmitter package pins.
Set Up	Lane5	Lane5	0.0, 1.0	Select tests performed at the transmitter package pins.
Set Up	Lane6	Lane6	0.0, 1.0	Select tests performed at the transmitter package pins.
Set Up	Lane7	Lane7	0.0, 1.0	Select tests performed at the transmitter package pins.
Set Up	Lane8	Lane8	0.0, 1.0	Select tests performed at the transmitter package pins.
Set Up	Lane9	Lane9	0.0, 1.0	Select tests performed at the transmitter package pins.
Set Up	Power Level	PowerLevel	Full, Half	Select the PCI Express device Power Level to use.
Set Up	Preset Tests For Gen 3	TestPoint_Calibration	0.0, 1.0	Select tests peformed at the reference clock interface.
Set Up	Receiver Tests	TestPoint_Receiver	0.0, 1.0	Select tests peformed at the receiver.
Set Up	RefClk Tests	TestPoint_RefClk	0.0, 1.0	Select tests peformed at the reference clock interface.
Set Up	SSC	persistentCheckBox_SSC	0.0, 1.0	Indicate whether Spread Spectrum Clock is used.
Set Up	SigTestVersion	SigTestVersion	(Accepts user-defined text)	SigTestVersion SigTestVersion
Set Up	System Board Tests	TestPoint_SystemBoard	0.0, 1.0	Select tests peformed at the add-in card interface on the system board transmitter path.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Transmitter Tests	TestPoint_Transmitter	0.0, 1.0	Select tests performed at the transmitter package pins.
Set Up	User Comments	txtUserComment	(Accepts user-defined text)	Optional user comments displayed in the test report.
Set Up	cmbPresetTyp e	cmbPresetType	(Accepts user-defined text), None, P0, P1, P2, P3, P5, P6, P7, P8, P9, P10	Connection Type
*Limited availability: Availability of this setting depends upon the oscilloscope model and installed license options.				

3 Test Names and IDs

The following table shows the mapping between each test's numeric ID and name. The numeric ID is required by various remote interface methods.

- Name – The name of the test as it appears on the user interface **Select Tests** tab.
- Test ID – The number to use with the RunTests method.
- Description – The description of the test as it appears on the user interface **Select Tests** tab.

For example, if the graphical user interface displays this tree in the **Select Tests** tab:

- All Tests
  - Rise Time
  - Fall Time

then you would expect to see something like this in the table below:

Table 3 Example Test Names and IDs

Name	Test ID	Description
Fall Time	110	Measures clock fall time.
Rise Time	100	Measures clock rise time.

and you would run these tests remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SelectedTests '100,110'"
arsl -a ipaddress -c "Run"

C# syntax
---------
remoteAte.SelectedTests = new int[]{100,110};
remoteAte.Run();
```

Here are the actual Test names and IDs used by this application:

NOTE The file, "TestInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 4 Test IDs and Names

Name	TestID	Description
Reference Clock, High frequency > 1.5MHz RMS Jitter (Data Clk) (PCIE 2.0, 5.0 GT/s)	2860	This test verifies that the reference clock TREFCLK-HF-RMS is less than the maximum allowed value.
Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Data Clk) (PCIE 2.0, 5.0 GT/s)	2880	This test verifies that the RMS reference clock phase jitter at a bit error rate of 10E-6 is less than the maximum allowed value.
Add-in Card Tx, Eye-Width (PCIE 1.0a)	203	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Add-in Card Tx, Eye-Width (PCIE 1.1)	1330	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Add-in Card Tx, Eye-Width (PCIE 2.0, 2.5 GT/s)	2330	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Add-in Card Tx, Eye-Width (PCIE 3.0, 8.0 GT/s)	3430	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] -[TJ at BER -12].
Add-in Card Tx, Eye-Width -3.5dB with crosstalk (PCIE 2.0, 5.0 GT/s)	2336	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [TJ at BER-12].
Add-in Card Tx, Eye-Width -3.5dB without crosstalk (PCIE 2.0, 5.0 GT/s)	2337	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [TJ at BER-12].
Add-in Card Tx, Eye-Width -6.0dB with crosstalk (PCIE 2.0, 5.0 GT/s)	2338	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Add-in Card Tx, Eye-Width -6.0dB without crosstalk (PCIE 2.0, 5.0 GT/s)	2339	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Add-in Card Tx, Maximum Deterministic Jitter -3.5dB with crosstalk (PCIE 2.0, 5.0 GT/s)	2392	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-9 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Add-in Card Tx, Maximum Deterministic Jitter -3.5dB without crosstalk (PCIE 2.0, 5.0 GT/s)	2393	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-9 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
Add-in Card Tx, Maximum Deterministic Jitter -6.0dB with crosstalk (PCIE 2.0, 5.0 GT/s)	2394	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-9 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
Add-in Card Tx, Maximum Deterministic Jitter -6.0dB without crosstalk (PCIE 2.0, 5.0 GT/s)	2395	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-9 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
Add-in Card Tx, Median to Max Jitter (PCIE 1.0a)	202	This test measures the maximum time between the jitter median and maximum deviation from the median. The specified and measured values are shown in picoseconds here.
Add-in Card Tx, Median to Max Jitter (PCIE 1.1)	1320	This test measures the maximum time between the jitter median and maximum deviation from the median. The specified and measured values are shown in picoseconds here.
Add-in Card Tx, Median to Max Jitter (PCIE 2.0, 2.5 GT/s)	2320	This test measures the maximum time between the jitter median and maximum deviation from the median. The specified and measured values are shown in picoseconds here.
Add-in Card Tx, Peak Differential Output Voltage (Non Transtion)(PCIE 3.0, 8.0 GT/s)	3421	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Add-in Card Tx, Peak Differential Output Voltage (NonTransition)(PCIE 1.1)	1350	This test verifies that the Peak Differential Output Voltage for non transition bits is within the allowed range.
Add-in Card Tx, Peak Differential Output Voltage (NonTransition)(PCIE 2.0, 2.5 GT/s)	2350	This test verifies that the Peak Differential Output Voltage for non transition bits is within the allowed range.
Add-in Card Tx, Peak Differential Output Voltage (PCIE 1.0a)	207	This test verifies that the Peak Differential Output Voltage is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Add-in Card Tx, Peak Differential Output Voltage (Transition)(PCIE 1.1)	1340	This test verifies that the Peak Differential Output Voltage for transition bits is within the allowed range.
Add-in Card Tx, Peak Differential Output Voltage (Transition)(PCIE 2.0, 2.5 GT/s)	2340	This test verifies that the Peak Differential Output Voltage for transition bits is within the allowed range.
Add-in Card Tx, Peak Differential Output Voltage (Transition)(PCIE 3.0, 8.0 GT/s)	3420	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Add-in Card Tx, Peak Differential Output Voltage -3.5dB (Non-Transition)(PCIE 2.0, 5.0 GT/s)	2356	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Add-in Card Tx, Peak Differential Output Voltage -3.5dB (Transition) (PCIE 2.0, 5.0 GT/s)	2346	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Add-in Card Tx, Peak Differential Output Voltage -6.0dB (Non Transition)(PCIE 2.0, 5.0 GT/s)	2358	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Add-in Card Tx, Peak Differential Output Voltage -6.0dB (Transition)(PCIE 2.0, 5.0 GT/s)	2348	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Add-in Card Tx, RMS Random Jitter -3.5dB with crosstalk (PCIE 2.0, 5.0 GT/s)	2382	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
Add-in Card Tx, RMS Random Jitter -3.5dB without crosstalk (PCIE 2.0, 5.0 GT/s)	2383	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
Add-in Card Tx, RMS Random Jitter -6.0dB with crosstalk (PCIE 2.0, 5.0 GT/s)	2384	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
Add-in Card Tx, RMS Random Jitter -6.0dB without crosstalk (PCIE 2.0, 5.0 GT/s)	2385	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Add-in Card Tx, Template Tests (PCIE 1.0a)	210	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-6 of section 4.7.1 of the PCI Express Card Electromechanical Specification (CEM) Rev 1.0a, as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in figure 4-8.
Add-in Card Tx, Template Tests (PCIE 1.1)	1310	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-7 of section 4.7.1 of the PCI Express Card Electromechanical Specification (CEM) Rev 1.1, as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in figure 4-8.
Add-in Card Tx, Template Tests (PCIE 2.0, 2.5 GT/s)	2310	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-7 of section 4.7.1 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in figure 4-6.
Add-in Card Tx, Template Tests (PCIE 3.0, 8.0 GT/s)	3410	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-11 of section 4.8.3 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
Add-in Card Tx, Template Tests -3.5dB (PCIE 2.0, 5.0 GT/s)	2316	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-8 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in figure 4-7.
Add-in Card Tx, Template Tests -6.0dB (PCIE 2.0, 5.0 GT/s)	2318	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-10 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in figure 4-7.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Add-in Card Tx, Total Jitter at BER-12 -3.5dB with crosstalk (PCIE 2.0, 5.0 GT/s)	2396	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-9 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
Add-in Card Tx, Total Jitter at BER-12 -3.5dB without crosstalk (PCIE 2.0, 5.0 GT/s)	2397	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-9 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
Add-in Card Tx, Total Jitter at BER-12 -6.0dB with crosstalk (PCIE 2.0, 5.0 GT/s)	2398	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-9 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
Add-in Card Tx, Total Jitter at BER-12 -6.0dB without crosstalk (PCIE 2.0, 5.0 GT/s)	2399	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-9 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
Add-in Card Tx, Unit Interval (PCIE 1.0a)	200	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
Add-in Card Tx, Unit Interval (PCIE 1.1)	1300	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
Add-in Card Tx, Unit Interval (PCIE 2.0, 2.5 GT/s)	2301	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
Add-in Card Tx, Unit Interval (PCIE 2.0, 5.0 GT/s)	2300	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Add-in Card Tx, Unit Interval (PCIE 3.0, 8.0 GT/s)	3400	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
ExpressCard Host Tx, Eye-Width (EC 1.0)	703	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
ExpressCard Host Tx, Median to Max Jitter (EC 1.0)	702	This test measures the maximum time between the jitter median and maximum deviation from the median. The specified and measured values are shown in picoseconds here.
ExpressCard Host Tx, Peak Differential Output Voltage (EC 1.0)	707	This test verifies that the Peak Differential Output Voltage is within the allowed range.
ExpressCard Host Tx, Template Tests (EC 1.0)	710	ExpressCard Hosts must meet the ExpressCard Host Transmitter Path Compliance Eye Requirements specified in table 4-5 of section 4.2.1 of the ExpressCard(TM) Standard, referenced to an ideal 100 ohm load at the end of the interconnect path at the isolated module connector pad boundary of an ExpressCard Module when mated with a connector.
ExpressCard Host Tx, Unit Interval (EC 1.0)	700	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
ExpressCard Module Tx, Eye-Width (EC 1.0)	603	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
ExpressCard Module Tx, Median to Max Jitter (EC 1.0)	602	This test measures the maximum time between the jitter median and maximum deviation from the median. The specified and measured values are shown in picoseconds here.
ExpressCard Module Tx, Peak Differential Output Voltage (EC 1.0)	607	This test verifies that the Peak Differential Output Voltage is within the allowed range.
ExpressCard Module Tx, Template Tests (EC 1.0)	610	ExpressCard Modules must meet the ExpressCard Module Transmitter Path Compliance Eye Requirements specified in table 4-3 of section 4.2.1 of the ExpressCard(TM) Standard, referenced to an ideal 100 ohm load at the end of the interconnect path at the module connector pad boundary.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
ExpressCard Module Tx, Unit Interval (EC 1.0)	600	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
No tests available	9999	
Reference Clock, Absolute Crossing Point Voltage (PCIE 1.1)	880	This test verifies that the absolute crossing point voltage of the reference clock single-ended waveforms is within the allowed range.
Reference Clock, Absolute Max Input Voltage (PCIE 1.1)	900	This test verifies that the absolute maximum input voltage of the reference clock is within the allowed range.
Reference Clock, Absolute Min Input Voltage (PCIE 1.1)	910	This test verifies that the absolute minimum input voltage of the reference clock is within the allowed range.
Reference Clock, Average Clock Period (PCIE 1.1)	860	The average clock period accuracy of the differential waveform is measured in PPM (parts per million) where 1 PPM equals 100Hz. A requirement of +/- 300 PPM applies to systems that do NOT employ SSC or that use a common clock source. For systems employing SSC there is an additional 2500 PPM nominal shift in the maximum period resulting in a maximum average period specification of +2800 PPM.
Reference Clock, Clock Frequency (Common Clk)(PCIE 3.0, 8.0 GT/s)	3810	This test verifies that the measured reference clock frequency, FREFCLK, is within than the allowed frequency range.
Reference Clock, Clock Frequency (Data Clk) (PCIE 3.0, 8.0 GT/s)	3860	This test verifies that the measured reference clock frequency, FREFCLK, is within than the allowed frequency range.
Reference Clock, Differential Input High Voltage (PCIE 1.1)	840	This test verifies that the high voltage of the reference clock differential waveform is greater than the minimum allowed value.
Reference Clock, Differential Input Low Voltage (PCIE 1.1)	850	This test verifies that the low voltage of the reference clock differential waveform is less than the maximum allowed value.
Reference Clock, Duty Cycle (PCIE 1.1)	870	This test verifies that the duty cycle of the reference clock differential waveform is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Reference Clock, Falling Edge Rate (PCIE 1.1)	830	This test verifies that the falling edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing.
Reference Clock, Full SSC Modulation (Data Clk) (PCIE 2.0, 5.0 GT/s)	2870	This test verifies that the reference clock full SSC modulation is less than the maximum allowed value.
Reference Clock, High frequency > 1.5MHz RMS Jitter (Common Clk) (PCIE 2.0, 5.0 GT/s)	2810	This test verifies that the reference clock TREFCLK-HF-RMS is less than the maximum allowed value.
Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Common Clk) (PCIE 2.0, 5.0 GT/s)	2830	This test verifies that the reference clock TREFCLK-LF-RMS is less than the maximum allowed value.
Reference Clock, Maximum SSC Slew Rate (Common Clk) (PCIE 2.0, 5.0GT/s)	2850	This test verifies that the reference clock SSC slew rate is less than the maximum allowed value.
Reference Clock, Maximum SSC Slew Rate (Data Clk) (PCIE 2.0, 5.0 GT/s)	2895	This test verifies that the reference clock SSC slew rate is less than the maximum allowed value.
Reference Clock, Phase Jitter (PCIE 1.1)	810	This test verifies that the magnitude of the peak-peak reference clock phase jitter at a bit error rate of 10E-6 is less than the maximum allowed value.
Reference Clock, RMS Jitter (Common Clk) (PCIE 3.0, 8.0 GT/s)	3820	This test verifies that the measured RMS jitter, TREFCLK-RMS-DC, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Data Clk) (PCIE 3.0, 8.0 GT/s)	3870	This test verifies that the measured RMS jitter, TREFCLK-RMS-DC, is less than the maximum allowed value.
Reference Clock, Rise-Fall Matching (PCIE 1.1)	920	This test verifies that the rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching is within the allowed range.
Reference Clock, Rising Edge Rate (PCIE 1.1)	820	This test verifies that the rising edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing.
Reference Clock, SSC Deviation (Common Clk) (PCIE 2.0, 5.0GT/s)	2840	This test verifies that the reference clock SSC deviation is less than the maximum allowed value.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Reference Clock, SSC Deviation (Common Clk) (PCIE 3.0, 8.0GT/s)	3840	This test verifies that the reference clock SSC deviation, TSSC-FREQ-DEVIATION, is less than the maximum allowed value.
Reference Clock, SSC Deviation (Data Clk) (PCIE 2.0, 5.0 GT/s)	2890	This test verifies that the reference clock SSC deviation is less than the maximum allowed value.
Reference Clock, SSC Deviation (Data Clk)(Min)(PCIE 3.0, 8.0GT/s)	3891	This test verifies that the reference clock SSC deviation, TSSC-FREQ-DEVIATION, is less than the maximum allowed value.
Reference Clock, SSC Deviation (Data Clk)(PCIE 3.0, 8.0GT/s)	3890	This test verifies that the reference clock SSC deviation, TSSC-FREQ-DEVIATION, is less than the maximum allowed value.
Reference Clock, SSC Deviation (Min)(Common Clk) (PCIE 2.0, 5.0GT/s)	2841	This test verifies that the reference clock SSC deviation is less than the maximum allowed value.
Reference Clock, SSC Deviation (Min)(Common Clk) (PCIE 3.0, 8.0GT/s)	3841	This test verifies that the reference clock SSC deviation, TSSC-FREQ-DEVIATION, is less than the maximum allowed value.
Reference Clock, SSC Deviation (Min)(Data Clk) (PCIE 2.0, 5.0 GT/s)	2891	This test verifies that the reference clock SSC deviation is less than the maximum allowed value.
Reference Clock, SSC Frequency Range (Common Clk) (PCIE 3.0, 8.0 GT/s)	3830	This test verifies that the measured SSC frequency, FSSC, is within the allowed SSC frequency range.
Reference Clock, SSC Frequency Range (Data Clk) (PCIE 3.0, 8.0 GT/s)	3880	This test verifies that the measured SSC frequency, FSSC, is within the allowed SSC frequency range.
Reference Clock, SSC Residual (Common Clk) (PCIE 2.0, 5.0 GT/s)	2820	This test verifies that the measured SSC residual is less than the maximum allowed value.
Reference Clock, Variation of VCross (PCIE 1.1)	890	This test verifies that the variation of VCross over all rising clock edges is within the allowed range.
Rx, AC Peak Common Mode Input Voltage (PCIE 1.0a)	108	Receivers must reliably receive data when there is less than 150 mV of AC (>30 kHz) peak common mode input voltage. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6 of the PCI Express Base Specification, Rev 1.0a.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Rx, AC Peak Common Mode Input Voltage (PCIE 1.1)	1250	Receivers must reliably receive data when there is less than 150 mV of AC (>30 kHz) peak common mode input voltage. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6 of the PCI Express Base Specification, Rev 1.1.
Rx, AC Peak Common Mode Input Voltage (PCIE 2.0, 2.5 GT/s)	2250	Receivers must reliably receive data when there is less than 150 mV of AC (>30 kHz) peak common mode input voltage. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12 of the PCI Express Base Specification, Rev 2.0.
Rx, Common RefClk Architecture Unit Interval (PCIE 2.0, 5.0 GT/s)	2202	A recovered RX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered RX UI is reported here. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in the PCI Express Base Specification.
Rx, Common Refclk Architecture Maximum Deterministic Jitter (PCIE 2.0, 5.0 GT/s)	2294	This test verifies that the Deterministic Jitter is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12.
Rx, Common Refclk Architecture Peak Differential Output Voltage (PCIE 2.0, 5.0 GT/s)	2243	This test verifies that the Peak Differential Output Voltage is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12.
Rx, Common Refclk Architecture RMS Random Jitter (PCIE 2.0, 5.0 GT/s)	2284	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
Rx, Common Refclk Architecture Template Test (PCIE 2.0, 5.0 GT/s)	2211	The receiver must reliably receive all data that meets the differential receiver input specifications as shown in Table 4-12 in the PCI Express Base Specification. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in Table 4-12.
Rx, Common Refclk Architecture Total Jitter at BER-12 (PCIE 2.0, 5.0 GT/s)	2298	This test verifies that the Total Jitter is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Rx, Data Clocked Architecture Maximum Deterministic Jitter (PCIE 2.0, 5.0 GT/s)	2292	This test verifies that the Deterministic Jitter is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12.
Rx, Data Clocked Architecture Peak Differential Output Voltage (PCIE 2.0, 5.0 GT/s)	2241	This test verifies that the Peak Differential Output Voltage is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12.
Rx, Data Clocked Architecture RMS Random Jitter (PCIE 2.0, 5.0 GT/s)	2282	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
Rx, Data Clocked Architecture Template Test (PCIE 2.0, 5.0 GT/s)	2210	The receiver must reliably receive all data that meets the differential receiver input specifications as shown in Table 4-12 in the PCI Express Base Specification. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in Table 4-12.
Rx, Data Clocked Architecture Total Jitter at BER-12 (PCIE 2.0, 5.0 GT/s)	2296	This test verifies that the Total Jitter is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12.
Rx, Data Clocked Architecture Unit Interval (PCIE 2.0, 5.0 GT/s)	2200	A recovered RX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered RX UI is reported here. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in the PCI Express Base Specification.
Rx, Eye-Width (PCIE 1.0a)	103	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter]. Note that this test does NOT test the receiver's tolerance. Rather, it test the quality of the signal as the receiver would see it. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6 of the PCI Express Base Specification, Rev 1.0a.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Rx, Eye-Width (PCIE 1.1)	1230	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter]. Note that this test does NOT test the receiver's tolerance. Rather, it test the quality of the signal as the receiver would see it. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6 of the PCI Express Base Specification, Rev 1.1.
Rx, Eye-Width (PCIE 2.0, 2.5 GT/s)	2230	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter]. Note that this test does NOT test the receiver's tolerance. Rather, it test the quality of the signal as the receiver would see it. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12 of the PCI Express Base Specification, Rev 2.0.
Rx, Long Channel CM Optimization (PCIE 3.0, 8.0 GT/s)	3695	This procedure minimizes the difference between the two components ofCM sinusoidal interference for Long Channel 8.0 Gbit/s.
Rx, Long Channel CM Sinusoidal Interference Calibration (PCIE 3.0, 8.0 GT/s)	3700	This procedure calibrates CM sinusoidal interference for Long Channel 8.0 Gbit/s.
Rx, Long Channel DM Sinusoidal Interference Calibration (PCIE 3.0, 8.0 GT/s)	3705	This procedure calibrates the differential mode sinusoidal interference for Long Channel 8.0 Gbit/s.
Rx, Long Channel Generator Launch Voltage Calibration (PCIE 3.0, 8.0 GT/s)	3690	This procedure calibrates the generator launch voltage for Long Channel 8.0 Gbit/s.
Rx, Long Channel Insertion Loss Calibration (PCIE 3.0, 8.0 GT/s)	3715	This procedure calculates the insertion loss at different de-emphasis levels for Long Channel 8.0 Gbit/s.
Rx, Long Channel Random Jitter Calibration (PCIE 3.0, 8.0 GT/s)	3710	This procedure calibrates random jitter for Long Channel 8.0 Gbit/s.
Rx, Long Channel Stressed Jitter Calibration (PCIE 3.0, 8.0 GT/s)	3730	
Rx, Long Channel Stressed Voltage Calibration (PCIE 3.0, 8.0 GT/s)	3720	This procedure calibrates the eye height for Long Channel 8.0 Gbit/s by adding CM differential interference at different launch voltage levels.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Rx, Median to Max Jitter (PCIE 1.0a)	102	Receivers must be able to reliably receive data with up to 120 ps between the jitter median and maximum deviation from the median. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6 of the PCI Express Base Specification, Rev 1.0a.
Rx, Median to Max Jitter (PCIE 1.1)	1220	Receivers must be able to reliably receive data with up to 120 ps between the jitter median and maximum deviation from the median. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6 of the PCI Express Base Specification, Rev 1.1.
Rx, Median to Max Jitter (PCIE 2.0, 2.5 GT/s)	2220	Receivers must be able to reliably receive data with up to 120 ps between the jitter median and maximum deviation from the median. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12 of the PCI Express Base Specification, Rev 2.0.
Rx, No Channel CM Optimization(PCIE 3.0, 8.0 GT/s)	3605	This procedure minimizes the difference between the two components of CM Sinusoidal Interference for No Channel 8.0 Gbit/s.
Rx, No Channel CM Sinusoidal Interference Calibration (PCIE 3.0, 8.0 GT/s)	3610	This procedure calibrates CM Sinusoidal Interference for No Channel 8.0 Gbit/s.
Rx, No Channel DM Sinusoidal Interference Calibration (PCIE 3.0, 8.0 GT/s)	3615	This procedure calibrates the differential mode sinusoidal interference for No Channel 8.0 Gbit/s.
Rx, No Channel Generator Launch Voltage Calibration(PCIE 3.0, 8.0 GT/s)	3600	This procedure calibrates the generator launch voltage for No Channel 8.0 Gbits/s.
Rx, No Channel Insertion Loss Calibration (PCIE 3.0, 8.0 GT/s)	3625	This procedure calculates the insertion loss at different de-emphasis levels for No Channel 8.0 Gbit/s.
Rx, No Channel Random Jitter Calibration (PCIE 3.0, 8.0 GT/s)	3620	The procedure calibrates random jitter for No Channel 8.0 Gbit/s.
Rx, No Channel Stressed Voltage Calibration (PCIE 3.0, 8.0 GT/s)	3630	This procedure calibrates the eye height for No Channel 8.0 GBit/s by adding CM differential interference at different launch levels.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Rx, Peak Differential Output Voltage (PCIE 1.0a)	107	This test verifies that the Peak Differential Output Voltage is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6.
Rx, Peak Differential Output Voltage (PCIE 1.1)	1240	This test verifies that the Peak Differential Output Voltage is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6.
Rx, Peak Differential Output Voltage (PCIE 2.0, 2.5 GT/s)	2240	This test verifies that the Peak Differential Output Voltage is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12.
Rx, Short Channel CM Optimization (PCIE 3.0, 8.0 GT/s)	3650	This procedure minimizes the difference between the two components of CM sinusoidal interference for Short Channel 8.0 Gbit/s.
Rx, Short Channel CM Sinusoidal Interference Calibration (PCIE 3.0, 8.0 GT/s)	3655	This procedure calibrates CM sinusoidal interference for Short Channel 8.0 GBit/s.
Rx, Short Channel DM Sinusoidal Interference Calibration (PCIE 3.0, 8.0 GT/s)	3660	This procedure calibrates the differential mode sinusoidal interference for Short Channel 8.0 Gbit/s.
Rx, Short Channel Generator Launch Voltage Calibration (PCIE 3.0, 8.0 GT/s)	3645	This procedure calibrates the generator launch voltage for Short Channel 8.0 Gbit/s.
Rx, Short Channel Insertion Loss Calibration (PCIE 3.0, 8.0 GT/s)	3670	This procedure calculates the insertion loss at different de-emphasis levels for Short Channel 8.0 Gbit/s.
Rx, Short Channel Random Jitter Calibration (PCIE 3.0, 8.0 GT/s)	3665	This procedure calibrates random jitter for Short Chanel 8.0 Gbit/s.
Rx, Short Channel Stressed Voltage Calibration (PCIE 3.0, 8.0 GT/s)	3675	This procedure calibrates the eye height for Short Channel 8.0 Gbit/s by adding CM differential interference at different launch voltage levels.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Rx, Template Test (PCIE 1.0a)	110	The receiver must reliably receive all data that meets the differential receiver input specifications as shown in Figure 4-26: Minimum Receiver Eye Timing and Voltage Compliance Specification as shown in the PCI Express Base Specification, Rev 1.0. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6.
Rx, Template Test (PCIE 1.1)	1210	The receiver must reliably receive all data that meets the differential receiver input specifications as shown in Figure 4-26: Minimum Receiver Eye Timing and Voltage Compliance Specification as shown in the PCI Express Base Specification, Rev 1.1. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6.
Rx, Template Test (PCIE 2.0, 2.5 GT/s)	2212	The receiver must reliably receive all data that meets the differential receiver input specifications in the PCI Express Base Specification, Rev 2.0. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12.
Rx, Unit Interval (PCIE 1.0a)	100	A recovered RX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered RX UI is reported here. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6 of the PCI Express Base Specification, Rev 1.0a.
Rx, Unit Interval (PCIE 1.1)	1200	A recovered RX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered RX UI is reported here. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6 of the PCI Express Base Specification, Rev 1.1.
Rx, Unit Interval (PCIE 2.0, 2.5 GT/s)	2201	A recovered RX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered RX UI is reported here. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications of the PCI Express Base Specification, Rev 2.0.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
System Board Tx, Total Jitter at BER-12 with crosstalk (PCIE 2.0, 5.0 GT/s)	2496	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-16 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.
System Board Tx, Total Jitter at BER-12 without crosstalk (PCIE 2.0, 5.0 GT/s)	2497	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-16 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.
System Board Tx, Eye-Width (PCIE 1.0a)	403	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
System Board Tx, Eye-Width (PCIE 1.1)	1430	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
System Board Tx, Eye-Width (PCIE 2.0, 2.5 GT/s)	2432	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
System Board Tx, Eye-Width (PCIE 3.0, 8.0 GT/s)	3530	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] -[TJ at BER -12].
System Board Tx, Eye-Width with crosstalk (PCIE 2.0, 5.0 GT/s)	2430	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
System Board Tx, Eye-Width without crosstalk (PCIE 2.0, 5.0 GT/s)	2431	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
System Board Tx, Maximum Deterministic Jitter with crosstalk (PCIE 2.0, 5.0 GT/s)	2492	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-16 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.
System Board Tx, Maximum Deterministic Jitter without crosstalk (PCIE 2.0, 5.0 GT/s)	2493	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-16 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
System Board Tx, Median to Max Jitter (PCIE 1.0a)	402	This test measures the maximum time between the jitter median and maximum deviation from the median.
System Board Tx, Median to Max Jitter (PCIE 1.1)	1420	This test measures the maximum time between the jitter median and maximum deviation from the median.
System Board Tx, Median to Max Jitter (PCIE 2.0, 2.5 GT/s)	2420	This test measures the maximum time between the jitter median and maximum deviation from the median.
System Board Tx, Peak Differential Output Voltage (Non Transition)(PCIE 2.0, 5.0 GT/s)	2450	This test verifies that the Differential Peak Differential Output Voltage is within the allowed range.
System Board Tx, Peak Differential Output Voltage (Non Transition)(PCIE 3.0, 8.0 GT/s)	3521	This test verifies that the Peak Differential Output Voltage is within the allowed range.
System Board Tx, Peak Differential Output Voltage (NonTransition)(PCIE 1.1)	1450	This test verifies that the Differential Peak Differential Output Voltage for non transition bits is within the allowed range.
System Board Tx, Peak Differential Output Voltage (NonTransition)(PCIE 2.0, 2.5 GT/s)	2442	This test verifies that the Peak Differential Output Voltage for non transition bits is within the allowed range.
System Board Tx, Peak Differential Output Voltage (PCIE 1.0a)	407	This test verifies that the Differential Peak Differential Output Voltage is within the allowed range.
System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 1.1)	1440	This test verifies that the Differential Peak Differential Output Voltage for transition bits is within the allowed range.
System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 2.0, 2.5 GT/s)	2441	This test verifies that the Peak Differential Output Voltage for transition bits is within the allowed range.
System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 2.0, 5.0 GT/s)	2440	This test verifies that the Differential Peak Differential Output Voltage is within the allowed range.
System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 3.0, 8.0 GT/s)	3520	This test verifies that the Peak Differential Output Voltage is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
System Board Tx, RMS Random Jitter with crosstalk (PCIE 2.0, 5.0 GT/s)	2482	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
System Board Tx, RMS Random Jitter without crosstalk (PCIE 2.0, 5.0 GT/s)	2483	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
System Board Tx, Template Tests (PCIE 1.0a)	410	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-8 of section 4.7.3 of the PCI Express Card Electromechanical (CEM) Specification, Rev 1.0a, as measured after the connector with an ideal load.
System Board Tx, Template Tests (PCIE 1.1)	1410	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-8 of section 4.7.3 of the PCI Express Card Electromechanical (CEM) Specification, Rev 1.1, as measured after the connector with an ideal load.
System Board Tx, Template Tests (PCIE 2.0, 2.5 GT/s)	2411	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-14 of section 4.7.5 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.
System Board Tx, Template Tests (PCIE 2.0, 5.0 GT/s)	2410	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-15 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.
System Board Tx, Template Tests (PCIE 3.0, 8.0 GT/s)	3510	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-19 of section 4.8.9 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
System Board Tx, Unit Interval (PCIE 1.0a)	400	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
System Board Tx, Unit Interval (PCIE 1.1)	1400	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
System Board Tx, Unit Interval (PCIE 2.0, 2.5 GT/s)	2401	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
System Board Tx, Unit Interval (PCIE 2.0, 5.0 GT/s)	2400	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
System Board Tx, Unit Interval (PCIE 3.0, 8.0 GT/s)	3500	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
Tx, AC Peak Common Mode Output Voltage (PCIE 2.0, 5.0 GT/s)	3170	The maximum allowable RMS AC (>30Khz) common mode voltage is 100mVpp (Vtx-cm-ac-pp) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, AC common mode voltage - 30kHz to 500MHz (PCIE 3.0, 8.0 GT/s)	3022	This test verify the AC common mode lies in the 0.03-500MHz range, VTX-CM-AC-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, AC common mode voltage - 4GHz LPF (PCIE 3.0, 8.0 GT/s)	3021	This test verify the AC common mode, VTX-CM-AC-PP (4GHz LPF) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, Absolute delta of DC common mode voltage between D+ and D- (PCIE 3.0, 8.0 GT/s)	3030	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Absolute delta of DC common mode voltage during L0 and Idle (PCIE 2.0, 5.0 GT/s)	2040	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE_IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.
Tx, Absolute delta of DC common mode voltage during L0 and Idle (PCIE 3.0, 8.0 GT/s)	3040	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE_IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.
Tx, Avg DC Common Mode Voltage (PCIE 1.0a)	6	This test measures VTX-DC-CM as specified in the PCI Express Base Specification, Rev 1.0a. This is the allowed DC Common Mode voltage under any conditions. The average DC Common Mode voltage is reported here.
Tx, Avg DC Common Mode Voltage (PCIE 1.1)	1180	This test measures VTX-DC-CM as specified in the PCI Express Base Specification, Rev 1.1. This is the allowed DC Common Mode voltage under any conditions. The average DC Common Mode voltage is reported here.
Tx, Avg DC Common Mode Voltage (PCIE 2.0, 2.5 GT/s)	2181	This test measures VTX-DC-CM as specified in the PCI Express Base Specification, Rev 2.0. This is the allowed DC Common Mode voltage under any conditions. The average DC Common Mode voltage is reported here.
Tx, Avg DC Common Mode Voltage (PCIE 2.0, 5.0 GT/s)	2180	This test measures VTX-DC-CM as specified in the PCI Express Base Specification. This is the allowed DC Common Mode voltage under any conditions. The average DC Common Mode voltage is reported here.
Tx, DC Common Mode Line Delta (PCIE 1.0a)	9	This test measures VTX-CM-DCLINE-DELTA as specified in Table 4-5 of the PCI Express Base Specification, Rev 1.0a. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, DC Common Mode Line Delta (PCIE 1.1)	1184	This test measures VTX-CM-DCLINE-DELTA as specified in Table 4-5 of the PCI Express Base Specification, Rev 1.1. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, DC Common Mode Line Delta (PCIE 2.0, 2.5 GT/s)	2185	This test measures VTX-CM-DCLINE-DELTA as specified in the PCI Express Base Specification, Rev 2.0. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, DC Common Mode Line Delta (PCIE 2.0, 5.0 GT/s)	2184	This test measures VTX-CM-DCLINE-DELTA as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, DC Common Mode Output Voltage Variation (PCIE 1.0a)	11	The TX DC common mode voltage must fixed within the range of 0 to 3.6 V during all states. Any variation of this fixed value must be within +\- 100 mV.
Tx, DC Common Mode Output Voltage Variation (PCIE 1.1)	1182	The TX DC common mode voltage must fixed within the range of 0 to 3.6 V during all states. Any variation of this fixed value must be within +\- 100 mV.
Tx, DC Common Mode Output Voltage Variation (PCIE 2.0, 2.5 GT/s)	2182	The TX DC common mode voltage must fixed within the range of 0 to 3.6 V during all states. Any variation of this fixed value must be within +\- 100 mV.
Tx, DC common mode voltage (PCIE 3.0, 8.0 GT/s)	3010	This test verify the DC common mode, VTX-CM-DC is within the allowed limit as specified in the PCI Express Base Specification.
Tx, Data dependent jitter (PCIE 3.0, 8.0 GT/s)	3130	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, De-emphasis Preset #0 (PCIE 3.0, 8.0 GT/s)	3220	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, De-emphasis Preset #1 (PCIE 3.0, 8.0 GT/s)	3210	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, De-emphasis Preset #10 (PCIE 3.0, 8.0 GT/s)	3300	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification. The P10 boost limits are not fixed. The allowable P10 boost range is defined by the coefficient space lying between the two diagonal lines in Figure 4-50 of the PCI Express Base Specification

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, De-emphasis Preset #2 (PCIE 3.0, 8.0 GT/s)	3290	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, De-emphasis Preset #3 (PCIE 3.0, 8.0 GT/s)	3280	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, De-emphasis Preset #7 (PCIE 3.0, 8.0 GT/s)	3250	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, De-emphasis Preset #8 (PCIE 3.0, 8.0 GT/s)	3240	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, Deemphasized Voltage Ratio (PCIE 1.0a)	5	This test measures the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition. The average de-emphasis value is tested against the specified value.
Tx, Deemphasized Voltage Ratio (PCIE 1.1)	1160	This test measures the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition. The average de-emphasis value is tested against the specified value.
Tx, Deemphasized Voltage Ratio (PCIE 2.0, 2.5 GT/s)	2160	This test measures the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition. The average de-emphasis value is tested against the specified value.
Tx, Deemphasized Voltage Ratio -3.5dB (PCIE 2.0, 5.0 GT/s)	2162	This test measures the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition. This measurement is for de-emphasis level settings of -3.5dB.
Tx, Deemphasized Voltage Ratio -6.0dB (PCIE 2.0, 5.0 GT/s)	2164	This test measures the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition. This measurement is for de-emphasis level settings of -6dB.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Determinisic DjDD uncorrelated PWJ (PCIE 3.0, 8.0 GT/s)	3120	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Deterministic Jitter > 1.5 MHz (PCIE 2.0, 5.0 GT/s)	2192	This test verifies that the high frequency(above 1.5MHz) Deterministic Jitter is within the allowed range.
Tx, Eye-Width (PCIE 1.0a)	3	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Tx, Eye-Width (PCIE 1.0a, Low Power)	10003	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Tx, Eye-Width (PCIE 1.1)	1130	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Tx, Eye-Width (PCIE 1.1, Low Power)	11130	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Tx, Eye-Width (PCIE 2.0, 2.5 GT/s)	2130	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Tx, Eye-Width (PCIE 2.0, 2.5 GT/s, Low Power)	12130	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Tx, Eye-Width (PCIE 2.0, 5.0 GT/s)	2134	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [TJ at BER-12].
Tx, Full swing Tx voltage with no TxEQ -Preset #4(PCIE 3.0, 8.0 GT/s)	3050	This test verifies that the full swing Tx voltage with no equalization VTX-FS-NO-EQ is within the allowed range.
Tx, Median to Max Jitter (PCIE 1.0a)	2	This test measures the maximum time between the jitter median and maximum deviation from the median.
Tx, Median to Max Jitter (PCIE 1.0a, Low Power)	10002	This test measures the maximum time between the jitter median and maximum deviation from the median.
Tx, Median to Max Jitter (PCIE 1.1)	1120	This test measures the maximum time between the jitter median and maximum deviation from the median.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Median to Max Jitter (PCIE 1.1, Low Power)	11120	This test measures the maximum time between the jitter median and maximum deviation from the median.
Tx, Median to Max Jitter (PCIE 2.0, 2.5 GT/s)	2120	This test measures the maximum time between the jitter median and maximum deviation from the median.
Tx, Median to Max Jitter (PCIE 2.0, 2.5 GT/s, Low Power)	12120	This test measures the maximum time between the jitter median and maximum deviation from the median.
Tx, Min swing during EIEOS for full swing (PCIE 3.0, 8.0 GT/s)	3070	This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range.
Tx, Min swing during EIEOS for reduced swing (PCIE 3.0, 8.0 GT/s, Low Power)	13080	This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range.
Tx, Peak Differential Output Voltage (Non Transition)(PCIE 1.0a)	70	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Non Transition)(PCIE 1.1)	11400	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Non Transition)(PCIE 2.0, 2.5 GT/s)	21400	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Non Transition)(PCIE 2.0, 5.0 GT/s)	2154	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Non Transition)(PCIE 2.0, 5.0 GT/s, Low Power)	21540	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (PCIE 1.0a, Low Power)	10007	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (PCIE 1.1, Low Power)	11140	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (PCIE 2.0, 2.5 GT/s, Low Power)	12140	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Transition) (PCIE 2.0, 5.0 GT/s)	2144	This test verifies that the Peak Differential Output Voltage is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Peak Differential Output Voltage (Transition) (PCIE 2.0, 5.0 GT/s, Low Power)	21440	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Transition)(PCIE 1.0a)	7	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Transition)(PCIE 1.1)	1140	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Transition)(PCIE 2.0, 2.5 GT/s)	2140	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Preshoot Preset #5 (PCIE 3.0, 8.0 GT/s)	3260	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, Preshoot Preset #6 (PCIE 3.0, 8.0 GT/s)	3270	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, Preshoot Preset #7 (PCIE 3.0, 8.0 GT/s)	3251	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, Preshoot Preset #8 (PCIE 3.0, 8.0 GT/s)	3241	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, Preshoot Preset #9 (PCIE 3.0, 8.0 GT/s)	3230	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, Pseudo package loss (PCIE 3.0, 8.0 GT/s)	3140	This test verifies that the maximum pseudo package loss, ps21TX is within the allowed range.
Tx, RMS AC Peak Common Mode Output Voltage (PCIE 1.0a)	8	The maximum allowable RMS AC (>30Khz) common mode voltage is 20mV (Vtx-cm-acp) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, RMS AC Peak Common Mode Output Voltage (PCIE 1.1)	1170	The maximum allowable RMS AC (>30Khz) common mode voltage is 20mV (Vtx-cm-acp) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, RMS AC Peak Common Mode Output Voltage (PCIE 2.0, 2.5 GT/s)	2170	The maximum allowable RMS AC (>30Khz) common mode voltage is 20mV (Vtx-cm-acp) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, Random Jitter < 1.5 MHz (PCIE 2.0, 5.0 GT/s)	2194	This test verifies that the low frequency(10kH to 1.5MHz) Random Jitter(rms) is within the allowed range.
Tx, Reduced swing Tx voltage with no TxEQ (PCIE 3.0, 8.0 GT/s, Low Power)	13060	This test verifies that the reduced swing Tx output voltage with no equalization VTX-RS-NO-EQ is within the allowed range.
Tx, Rise/Fall Time (PCIE 1.0a)	4	This test verifies that the minimum rise and fall time (on both D+ and D- separately) is no less than the specified value. An oscilloscope and probe with at least 10GHz bandwidth is recommended for accurate characterization of PCI-Express rise times less than 50ps. If the number is close to the specified value, you may need to verify this measurement with a higher bandwidth oscilloscope.
Tx, Rise/Fall Time (PCIE 1.1)	1150	This test verifies that the minimum rise and fall time (on both D+ and D- separately) is no less than the specified value. An oscilloscope and probe with at least 10GHz bandwidth is recommended for accurate characterization of PCI-Express rise times less than 50ps. If the number is close to the specified value, you may need to verify this measurement with a higher bandwidth oscilloscope.
Tx, Rise/Fall Time (PCIE 2.0, 2.5 GT/s)	2151	This test verifies that the minimum rise and fall time (on both D+ and D- separately) is no less than the specified value. An oscilloscope and probe with at least 10GHz bandwidth is recommended for accurate characterization of PCI-Express rise times less than 50ps. If the number is close to the specified value, you may need to verify this measurement with a higher bandwidth oscilloscope.
Tx, Rise/Fall Time (PCIE 2.0, 5.0 GT/s)	2150	This test verifies that the minimum rise and fall time (on both D+ and D- separately) is no less than the specified value. An oscilloscope and probe with at least 13GHz bandwidth is recommended for accurate characterization of PCI-Express rise times less than 50ps. If the number is close to the specified value, you may need to verify this measurement with a higher bandwidth oscilloscope.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Template Tests (PCIE 1.0a)	10	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification, Rev 1.0a, Section 4.3.3.1, Figure 4-24: Minimum Transmitter Timing and Voltage Output Compliance Specifications as measured at the package pins into the Compliance Test and Measurement Load, defined in section 4.3.3.2
Tx, Template Tests (PCIE 1.0a, Low Power)	10010	All PCI Express Device Types must meet the Transmitter eye diagram as specified in Mobile Graphic Low Power Addendum to The PCIE Base Specification 1.0, Figure 2.2
Tx, Template Tests (PCIE 1.1)	1110	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification, Rev 1.1, Section 4.3.3.1, Figure 4-24: Minimum Transmitter Timing and Voltage Output Compliance Specifications as measured at the package pins into the Compliance Test and Measurement Load, defined in section 4.3.3.2
Tx, Template Tests (PCIE 1.1, Low Power)	11110	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the Mobile Graphic Low Power Addendum to The PCIE Base Specification 1.0, Figure 2.2
Tx, Template Tests (PCIE 2.0, 2.5 GT/s)	2110	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification.
Tx, Template Tests (PCIE 2.0, 2.5 GT/s, Low Power)	12110	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification
Tx, Template Tests (PCIE 2.0, 5.0 GT/s)	2114	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification.
Tx, Template Tests (PCIE 2.0, 5.0 GT/s, Low Power)	21140	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification.
Tx, Tmin-Pulse (PCIE 2.0, 5.0 GT/s)	2152	This test verifies that the minimum pulse width is no less than the specified value. An oscilloscope and probe with at least 13GHz bandwidth is recommended for accurate characterization of PCI-Express rise times less than 50ps. If the number is close to the specified value, you may need to verify this measurement with a higher bandwidth oscilloscope.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Total uncorrelated PWJ (PCIE 3.0, 8.0 GT/s)	3110	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Uncorrelated deterministic jitter (PCIE 3.0, 8.0 GT/s)	3100	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated total jitter (PCIE 3.0, 8.0 GT/s)	3090	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Unit Interval (PCIE 1.0a)	1	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here.
Tx, Unit Interval (PCIE 1.1)	1100	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here.
Tx, Unit Interval (PCIE 2.0, 2.5 GT/s)	2101	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here.
Tx, Unit Interval (PCIE 2.0, 5.0 GT/s)	2100	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here.
Tx, Unit interval (PCIE 3.0, 8.0 GT/s)	3000	The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 4-19 of the PCI Express Base Specification.

4 Instruments

The following table shows the instruments used by this application. The name is required by various remote interface methods.

- Instrument Name — The name to use as a parameter in remote interface commands.
- Description — The description of the instrument.

For example, if an application uses an oscilloscope and a pulse generator, then you would expect to see something like this in the table below:

Table 5 Example Instrument Information

Name	Description
scope	The primary oscilloscope.
Pulse	The pulse generator used for Gen 2 tests.

and you would be able to remotely control an instrument using:

```
ARSL syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
arsl -a ipaddress -c "SendScpiCommandCustom 'Command=[scpi
command];Timeout=100;Instrument=pulsegen'"

arsl -a ipaddress -c "SendScpiQueryCustom 'Command=[scpi
query];Timeout=100;Instrument=pulsegen'"


C# syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
SendScpiCommandOptions commandOptions = new SendScpiCommandOptions();
commandOptions.Command = "[scpi command]";
commandOptions.Instrument = "[instrument name]";
commandOptions.Timeout = [timeout];
remoteAte.SendScpiCommand(commandOptions);

SendScpiQueryOptions queryOptions = new SendScpiQueryOptions();
queryOptions.Query = "[scpi query]";
queryOptions.Instrument = "[instrument name]";
```

```
queryOptions.Timeout = [timeout];
remoteAte.SendScpiQuery(queryOptions);
```

Here are the actual instrument names used by this application:

NOTE The file, "InstrumentInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 6 Instrument Names

Instrument Name	Description
81150A	81150A
N4903B	N4903B
scope	The primary oscilloscope

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